F0056/1663P PATENT

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Zoran Krivokapic

Serial No.: 09/592,124

Filed: June 12, 2000

Group Art Unit: 2823

Before the Examiner: Pham, Long

Title: METHOD AND SYSTEM FOR FORMING A LONG CHANNEL DEVICE

SUPPLEMENTAL APPEAL BRIEF

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is being submitted pursuant to 37 C.F.R. §1.193(b)(2)(ii). Appellant is furnishing herewith three (3) copies of this brief.

CERTIFICATION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 20, 2003.

Serena Beller
Signature

Serena Beller
(Printed name of person certifying)

I. INCORPORATION BY REFERENCE

The Appellant hereby incorporates herein by reference Sections I-V and VII-IX of Appellant's Brief mailed on January 27, 2003.

II. ISSUE

A. Are claims 9-16 properly rejected under 35 U.S.C. §103(a) as being unpatenable over Dennison et al. (U.S. Patent No. 6,004,854) (hereinafter "Dennison")?

III. ADDITIONAL ARGUMENT

A. Claims 9-16 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Dennison.

The Examiner has rejected claims 9-16 under 35 U.S.C. §103(a) as being unpatenable over Dennison. Paper no. 12, pages 2-3.

1. The Examiner Has Not Presented a *Prima Facie* Case of Obviousness

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re* Lee, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

> With regard to the obviousness rejections, the Examiner states:
>
> Dennison et al. teach forming the plurality of gate structures on a single active region 12 but *fail to teach that the active region is formed on a substrate as recited in claim 9.* However, the formation of devices on an active region on a substrate is well-known. Paper No. 12, page 3.

Thus, the Examiner is simply relying on his own subjective opinion in support of modifying Dennison to form "an active region on a substrate," as recited in claim 9. The Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Dennison to form an active region on a substrate. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 9-16. M.P.E.P. §2143.

> The Examiner further states:
>
> Dennison teaches each of the three gate structures comprises length and disposed at a distance apart, *but fails to teach the range for the channel length and separated distance as recited in present claim 12.* However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal range for the channel length and separated distance through routine experimentation and optimization to obtain optimal or desired device performance. Paper No. 12, pages 3-4.

Thus, the Examiner's motivation for modifying Dennison to provide an active region on a substrate comprising three gate structures "where each of the three gate structures comprises a channel length of at least 0.13 μm disposed at least 0.2μm apart," as recited in claim 12, is "because it would have been obvious to one ordinary skill in the art of making semiconductor devices to determine the workable or optimal range for the channel length and separated distance through routine experimentation and optimization to obtain optimal or desired device performance." Paper No. 12, pages 3-4.

If the Examiner is asserting that one of ordinary skill in the art would know to modify Dennison to provide an active region on a substrate comprising three gate structures "where each of the three gate structures comprises a channel length of at least 0.13 μm disposed at least 0.2μm apart," as recited in claim 12, then the Examiner must present evidence as to what is the level of ordinary skill in the art. M.P.E.P. §2143.03. The Examiner has not presented any evidence of considering the factors to determine the level of ordinary skill in the art such as (1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field. *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696, 218 U.S.P.Q. 865, 868 (Fed. Cir. 1983); M.P.E.P. §2141.03.

Further, the Examiner has not shown why Dennison should be modified to provide an active region on a substrate comprising three gate structures. Further, the Examiner has not shown why Dennison should be modified to provide an active region on a substrate comprising three gate structures where each of the three gate structures comprises a channel length of at least 0.13 μm disposed at least 0.2μm apart. The Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying Dennison to provide an active region on a substrate comprising three gate structures where each of the three gate structures comprises a channel length of at least 0.13 μm disposed at least 0.2μm apart. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). The Examiner simply states that one of ordinary skill of making semiconductor devices would determine the workable or optimal range for the channel length and separated distance through routine experimentation and optimization to obtain optimal or desired device performance. The Examiner has not presented any evidence for supporting the proposition that one of ordinary skill in the art would determine to modify Dennison to provide an active

region on a substrate comprising three gate structures where each of the three gate structures comprises a channel length of at least 0.13 μm disposed at least 0.2μm apart simply from experimentation. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 12. M.P.E.P. §2143.

2. Dennison does not Teach or Suggest the Following Claim Limitations

Dennison does not teach "means for providing an active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures" as recited in claim 9. The Examiner directs Appellant's attention to elements 12, 16, 20 and 24 in Figure 1 as disclosing the above-cited claim limitation. Paper No. 6, page 2. Instead, Dennison teaches:

> Providing a series of gate lines over a semiconductor substrate, the gate lines comprising memory array gate lines and peripheral circuitry gate lines, a first gate line being positioned relative to a first peripheral area of the substrate for formation of a peripheral NMOS transistor, a second gate line being positioned relative to a second peripheral area of the substrate for formation of a peripheral PMOS transistor, a third gate line being positioned relative to a memory array area of the substrate for formation of a memory array NMOS transistor. Column 2, Lines 20-29.

> A first gate line 16 is positioned relative to a first peripheral area 18 of substrate 12 for formation of a peripheral NMOS transistor. A second gate line 20 is positioned relative to a second peripheral area 22 of substrate 12 and n-well 14 for formation of a peripheral PMOS transistor. A third gate line 24 is positioned relative to a memory array area 26 for formation of a memory array NMOS transistor. Column 3, Lines 19-25.

Thus, Dennison teaches *three gate lines on* ***three*** *active regions* (gate line 16 on a first active region 18, gate line 20 on a second active region 22 and gate line 24 on a third active region 26). As stated in Appellant's response with a mailing date of May 14, 2002,

> Active regions are regions that are defined on the substrate via a LOCOS (Local Oxidation of Silicon) or similar process upon which gate stacks are formed. These active regions are separated by isolation regions that are typically formed by growing a thin field oxide region (FOX) between the active regions using a thermal oxidation process. As a result, a plurality of active regions are formed on a single active region. Paper No. 7, Page 4.

Hence, Dennison does not teach a single active region on a substrate comprising a plurality of discontinuous gate structures. Instead, Dennison teaches three active regions on the substrate. Nowhere does Dennison teach or even suggest that these active regions could all be sub-regions of an active region.

The Examiner in response to Appellant's arguments states:

> It is noted that appellant's invention appears to be forming multiple gates on a single active region in a substrate. However, this is not what is recited in appealed claim 9. Claim 9 recites that 'the active region comprises a plurality of discontinuous gate structures'. The recitation of 'comprises' in the limitation allows inclusion of other elements such as other active regions or sub-regions on the active region on substrate 12. Although, Dennison teaches that multiple gates are formed on different active regions and/or wells, all of the active regions and/or well are formed on a single active region or substrate 12. See fig. 1 of Dennison. Paper No. 12, page 4.

Appellant disagrees. The Examiner is transmogrifying the claim language. Claim 9 states in part "providing an active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures." While the term "comprises" allows the inclusion of other elements, the claim refers to a single active region. The term "comprises" is not before the term "an active region" but instead follows the term "an active region." Hence, the Examiner is improperly interpreting claim 9 by

interpreting claim 9 as including multiple active regions.[1] M.P.E.P. §2111. Further, claim 9 specifically states "an active region on a substrate." It is improper for the Examiner to interpret substrate 12 as a single active region. M.P.E.P. §2111. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 9. M.P.E.P. §2143.

In response to Appellant's argument presented in Paper No. 7, the Examiner states:

> It is submitted that claims as written do not exclude the possibility that the active region have sub-regions. Note that the claims are given the broadest reasonable interpretation consistent with the specification during patent examination. See In re Morris, 127 F.3d 1048, 44 USPQ2d 1023 (Fed. Cir. 1997). Paper No. 8, page 3.

Appellant respectfully points out to the Examiner that the Examiner is entitled to give claim limitations their broadest reasonable interpretation *in light of the specification*. *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997); M.P.E.P. §2111-§2116.01. The Examiner cannot transmogrify the meaning of a claim in order to find a reference to reject the claim. In particular, the Examiner may not simply ignore language in the claims. All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); M.P.E.P. §2143.03. The claim states *an active region* that comprises a plurality of discontinuous gate structures which is supported at least in part on page 5, line 16 to page 6, line 10 and Figures 4-5 of Appellant's Specification. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 9. M.P.E.P. §2143.

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1 On July 29, 2003, Appellant had a telephonic interview with the Examiner in which an analogous claim limitation ("a bike comprising a plurality of wheels") was presented to the Examiner. The Examiner insisted that it was proper claim interpretation to interpret "a bike comprising a plurality of wheels" to read on two unicycles where each unicycle has a single wheel. Again, Appellant asserts that the Examiner is mistaken as the claim states a single bike and not a plurality of bikes where the single bike comprises a plurality of wheels.

Dennison does not teach or suggest "means for masking the plurality of gate structures prior to the ion implantation" as recited in claim 10. The Examiner directs Appellant's attention to element 38 as teaching the masking layer over the plurality of gate structures. Paper No. 6, page 2. Further, as stated above, the Examiner asserts that the plurality of gate structures corresponds to elements 16, 20 and 24. Paper No. 6, page 4. Instead, Dennison teaches:

> Referring to FIG. 2 a photoresist masking layer 38 is provided over second gate line 20, second peripheral PMOS substrate area 22, third gate line 24, and memory array NMOS substrate area 26. An n-type LDD implant 42, preferably As, is then provided into the exposed first peripheral NMOS substrate area 18 adjacent first gate line 16. Column 3, Lines 36-41.

Hence, Dennison teaches providing a photoresist masking layer only over two of the three gate lines (gate lines 20 and 24 and not gate line 16). Further, Dennison teaches implanting an LDD implant into the exposed substrate area 18. Thus, using the Examiner's definition of a plurality of gate structures corresponding to gate lines 16, 20 and 24, Dennison does not teach a photoresist masking layer over the plurality of gate structures prior to the ion implantation but only over a portion of the plurality of gate structures.

The Examiner in response to Appellant's arguments states:

> However, it is noted that 'plurality of gate structures' means at least two gate structures. With this interpretation, Dennison teaches masking the plurality of gate structures prior to the ion implantation as recited in present claim 10. See fig. 2 of Dennison. Paper No. 12, page 4.

Appellant disagrees. The Examiner is transmogrifying the claim language. The claim states "masking the plurality of gate structures" where the "plurality of gate structures" refers to the "plurality of discontinuous gate structures" that the "active region comprises." Hence, the claim states that the entire plurality of discontinuous gate structures are masked. The claim does not state a portion or a subset of the

plurality of discontinuous gate structures are masked as asserted by the Examiner.[2] Hence, the Examiner's claim interpretation is improper. M.P.E.P. §2111. The Examiner asserts that Dennison teaches that gate lines 16, 20 and 24 read on the limitation of "the plurality of discontinuous gate structures." Dennison teaches providing a photoresist masking layer only over two of the three gate lines. Hence, Dennison does not teach masking the plurality of gate structures. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 10. M.P.E.P. §2143.

Dennison does not teach "wherein the active region comprises three gate structures" as recited in claim 11. The Examiner directs Appellant's attention to elements 12, 16, 20 and 24 in Figure 1 as teaching the above-cited claim limitation. Paper No. 6, page 2. Instead, as stated above, Dennison teaches *three gate lines on three active regions* (gate line 16 on a first active region 18, gate line 20 on a second active region 22 and gate line 24 on a third active region 26). As stated above, active regions are regions that are defined on the substrate via a LOCOS (Local Oxidation of Silicon) or similar process upon which gate stacks are formed. These active regions are separated by isolation regions that are typically formed by growing a thin field oxide region (FOX) between the active regions using a thermal oxidation process. Hence, Dennison does not teach a single active region on a substrate comprising three gate structures. Instead, Dennison teaches three active regions on the substrate. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 11. M.P.E.P. §2143.

As a result of the foregoing, Appellant respectfully asserts that since there are numerous claim limitations not taught or suggested in the cited prior art, the

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2 If, however, claim 10 states "a plurality of the plurality of gate structures," then the Examiner's interpretation would be correct. However, claim 10 states "means for masking the plurality of gate structures prior to the ion implantation."

Examiner has not presented a *prima facie* case of obviousness for rejecting claims 9-16 in view of the cited prior art. M.P.E.P. §2143.

Respectfully submitted,
WINSTEAD SECHREST & MINICK P.C.
Attorneys for Appellant

By: _____
Robert A. Voigt, Jr.
Reg. No. 47,159
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
1201 Main Street
Dallas, Texas 75250-0784
(512) 370-2832

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